US-PAT-NO: 5826048
DOCUMENT-IDENTIFIER: US 5826048 A

TITLE: PCI bus with reduced number of signals

DATE-ISSUED: October 20, 1998

INVENTOR-INFORMATION:

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US-CL-CURRENT: 710/306

ABSTRACT:

A **Mini-PCI** (MPCI) interface, and associated circuits and methods are provided for connecting a Peripheral Component Interconnect (**PCI**) device to one or more external devices. The MPCI interface, circuits and methods provide for a substantial if not full implementation of a PCI Local Bus without requiring the standard number of pins, traces, or signals. The MPCI interface includes a PCI/MPCI bridge connected between a PCI bus and to up to eight external devices in the form of MPCI devices and linear memory devices. The PCI/MPCI bridge is capable of receiving an incoming PCI transaction and multiplexing some of its signals together to create a corresponding incoming MPCI transaction. This incoming MPCI transaction may then be passed over an MPCI bus, having fewer lines and optimally operating at a higher frequency, the external devices. The process is reversed for outgoing transactions, i.e., the MPCI transactions are de-multiplexed to create PCI transactions. Additionally, the MPCI interface may also be configured to provide for direct access to linearly addressed memory devices without adding a PCI interface to the external interface. The invention may be implemented through integrated circuitry and/or computer implemented instructions, and may be included within a personal computer.

22 Claims, 12 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

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Abstract Text - ABTX:

A **Mini-PCI** (MPCI) interface, and associated circuits and methods are provided for connecting a Peripheral Component Interconnect (**PCI**) device to one or more external devices. The MPCI interface, circuits and methods provide for a substantial if not full implementation of a PCI Local Bus without requiring the standard number of pins, traces, or signals. The MPCI interface includes a PCI/MPCI bridge connected between a PCI bus and to up to eight external devices in the form of MPCI devices and linear memory devices. The PCI/MPCI bridge is capable of receiving an incoming PCI transaction and multiplexing some of its signals together to create a corresponding incoming MPCI transaction. This incoming MPCI transaction may then be passed over an MPCI bus, having fewer lines and optimally operating at a higher frequency, the external devices. The process is reversed for outgoing transactions, i.e., the MPCI transactions are de-multiplexed to create PCI transactions. Additionally, the MPCI interface

may also be configured to provide for direct access to linearly addressed memory devices without adding a PCI interface to the external interface. The invention may be implemented through integrated circuitry and/or computer implemented instructions, and may be included within a personal computer.

Brief Summary Text - BSTX:

The present invention relates to, in one embodiment, a **Mini-PCI** (MPCI) interface for connecting a **PCI** bus to one or more external devices. The external devices can include MPCI devices, PCI devices and non-PCI devices such as linear memory addressed devices. The MPCI interface allows substantial implementation of a PCI Local Bus Specification while requiring fewer pins/signals.

Drawing Description Text - DRTX:

FIG. 2 is a block diagram of one embodiment, in accordance with the present invention, of a PCI/MPCI Bridge coupled to a **PCI** Local bus and a **Mini-PCI** (MPCI) bus which is further coupled to a plurality of MPCI and linear memory devices;

Detailed Description Text - DETX:

In accordance with one embodiment of the present invention there is provided a **Mini-PCI** (MPCI) interface that supports **PCI** compliant inputs and outputs with a reduced number of pins/signals. The MPCI interface can be used to couple a PCI bus to one or more external devices. The external devices can include specifically designed MPCI devices, PCI compliant devices or even linear addressed devices, such as a read only memory (ROM), or like device. The MPCI interface basically reduces the number of pins/signals required to complete a PCI transaction by providing a time-division multiplexed signaling scheme that can be controlled via one or more selected signals within the original PCI transaction.